Amendments to the Claims:

Please cancel claims 14 and 15.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

Claim 1 (previously presented): A method of performing additive synthesis of digital audio signals in a recursive digital oscillator, comprising:

receiving digital audio signal frames wherein each digital audio signal frame includes a set of frequency, amplitude, and phase components represented as coefficients of variables in a mathematical expression, each digital audio signal frame thereby including a frequency coefficient representation;

forming converted frequency coefficients by Re-Mapping of bits of said frequency coefficient representation to bias audio reproduction accuracy toward low frequency signals

wherein said digital oscillator is an oscillator as in claim 16 and wherein said Re-Mapping biases the generating frequency of said oscillator as in claim 17; and

performing additive synthesis with said converted frequency coefficients.

Claim 2 (previously presented): The method of claim 1 further comprising the step of defining said frequency coefficient representation with an exponent characterizing a floating-point range extension.

Claim 3 (previously presented): The method of claim 2 wherein said defining step includes the step of specifying said exponent to correspond to a right shift amount necessary to correct for precision limitations introduced by limiting Re-Mapping coefficients to 16 bits.

Claim 4 (previously presented): The method of claim 3 wherein said receiving, forming, and performing steps are implemented utilizing a 16-bit fixed point processor.

Claim 5 (previously presented): The method of claim 1 wherein said receiving, forming and performing steps are implemented utilizing a digital signal processor.

Claim 6 (previously presented): The method of claim 1 wherein said receiving, forming, and performing steps are implemented utilizing a field programmable gate array.

Claim 7 (previously presented): The method of claim 1 wherein said receiving, forming, and performing steps are implemented utilizing a Very Long Instruction Word processor.

Claim 8 (previously presented): The method of claim 1 wherein said receiving, forming, and performing steps are implemented utilizing a Reduced Instruction Set Computer.

Claim 9 (previously presented): The method of claim 1 wherein said receiving, forming, and performing steps are implemented utilizing a Residue Number System processor.

Claim 10 (previously presented): A computer readable memory to direct a processor to function in a specified manner, comprising:

a first set of executable instructions to receive digital audio signal frames wherein each digital audio signal frame has a set of specified frequency values expressed as a bit sequence;

a second set of executable instructions to Re-Map said bit sequence to represent lower frequencies with more significant bits and higher frequencies with less significant bits; and

a third set of executable instructions to facilitate additive synthesis of said digital audio signal frames in a reduced-precision recursive digital oscillator wherein said digital oscillator is an oscillator as in claim 16 and wherein said Re-Mapping biases the generating frequency of said oscillator as in claim 17.

Claim 11 (previously presented): The computer readable memory of claim 10 wherein said first set of executable instructions include instructions to identify a frequency coefficient representation of said specified frequency.

Claim 12 (previously presented): The computer readable memory of claim 11 further comprising a fourth set of executable instructions to define said frequency coefficient representation with an exponent characterizing a floating-point range extension.

Claim 13 (previously presented): The computer readable memory of claim 12 wherein said fourth set of executable instructions include instructions to specify said exponent

to correspond to a right shift amount necessary to correct for precision limitations introduced by a reduced precision processor.

Claims 14-15 (canceled)

Claim 17 (previously presented): An oscillator as in claim 16 wherein ε is represented by an unsigned mantissa, m, combined with an unsigned exponent, e, biased so that the actual represented value is

$$\varepsilon = 2^{2-e} m.$$

Claim 18 (previously presented): An oscillator as in claim 17 wherein said mantissa m is 16 bits.